Listing and Amendments to the Claims

This listing of claims will replace the claims that were published in the PCT Application and the International Preliminary Examination Report:

1. (currently amended) Data link layer device for a serial communication bus, in particular IEEE1394 bus, comprising an interface ~~(35)~~ to a physical layer unit ~~(20)~~ and an interface to at least one host processor supporting the higher layers of the OSI/ISO data communication reference model, ~~characterized in that~~ wherein, the data link layer device further comprises means ~~(31b)~~ for checking whether a cycle master capable of transmitting a cycle start packet determining minimum start times for isochronous and asynchronous data transmissions over the serial communication bus exists in the network and if not activating configuration means ~~(38)~~ that enable the generation of asynchronous transmission requests without waiting for a cycle start packet and an isochronous data transfer in order to support a no cycle master transfer mode.

2. (currently amended) Data link layer device according to claim 3 wherein the means for checking whether a cycle master exists in the network comprise a memory ~~(37)~~ storing the self-identification packets from all the nodes in the network and evaluating means for checking whether in one of the self-identification packets an entry is found that indicated that the corresponding node is contender for an isochronous resource manager ~~(42)~~.

3. (currently amended) Data link layer device according to claim 3, wherein the means for checking whether a cycle master exists in the network comprise a first counter ~~(31a)~~ counting clock pulses of a reference clock, the counter generating a cycle synchronization event each time after a predetermined counting interval, and comprising a second counter that is incremented each time that no cycle start packet has been received in succession to a cycle synchronization event, thereby activating said configuration means if the second counter reaches a predetermined value.

4. (currently amended) Data link layer device according to claim 3 wherein the means for checking whether a cycle master exists in the network comprise a memory ~~(37)~~ storing the self-identification packets from all the nodes in the network and evaluating means for checking whether in one of the self-identification packets an entry is found that indicated that the corresponding node is contender for an isochronous resource manager ~~(42)~~.

5. (currently amended) Data link layer device according to claim 3, wherein the means for checking whether a cycle master exists in the network comprise a first counter ~~(31a)~~ counting clock pulses of a reference clock, the counter generating a cycle synchronization event each time after a predetermined counting interval, and comprising a second counter that is incremented each time that no cycle start packet has been received in succession to a cycle synchronization event, thereby activating said configuration means if the second counter reaches a predetermined value.